ABSTRACT OF THE DISCLOSURE

A method or process of manufacturing on-chip capacitors on a VLSI device (or chip) is improved by utilizing a high-dielectric constant metal-insulator-metal (MIM) capacitor manufacturing process. The high-k constant MIM capacitor may include a lower electrode in a first metal layer of a VLSI device, a substantially thin layer of high-k insulator (e.g., silicon nitride at an interface of the first metal layer and a via, and an upper electrode form in a second metal layer. The via provides a channel between the second metal layer to the high-k insulator. The on-chip capacitors may be fabricated in a variety of configurations such as a parallel line, parallel plate or in a cross-over area of two different metal lines.